What Is Claimed Is:

1. A packaged semiconductor, comprising:

a semiconductor chip having a planar upper surface, a circumference and a bottom surface;

a plurality of input bond pads on the planar upper surface of said semiconductor chip along the circumference and electrically connected to said semiconductor chip;

a plurality of output bond pads on the planar upper surface along the circumference of said semiconductor chip and electrically connected to said semiconductor chip;

a leadframe having a plurality of tie bars, said tie bars having a side surface and a bottom surface, said leadframe having a plurality of dam bars;

a plurality of internal leads connected to said leadframe, said plurality of internal leads having a side surface and a bottom surface, said plurality of internal leads being radially formed at regular intervals along and spaced apart from said circumference of said semiconductor chip and extending towards said semiconductor chip, each of said plurality of internal leads having a half-etched section facing said semiconductor chip, each of said plurality of leads having an upper surface in the plane of said upper surface of said semiconductor chip;

a plurality of conductive wires for electrically connecting to said plurality of internal leads and to said semiconductor chip;

encapsulant material encapsulating said semiconductor chip, said plurality of conductive wires, and said plurality of internal leads to form a package body, wherein flow of said encapsulant material is limited by said plurality of dam bars formed on said leadframe; and

wherein said semiconductor chip, said plurality of internal leads and said plurality of tie bars are externally exposed at respective side and bottom surface.

2. The semiconductor package of claim 1, further comprising

a chip paddle connected to said leadframe, said chip paddle having a top surface, a side surface and a bottom surface, said chip paddle bonded to said bottom surface of said semiconductor chip by an adhesive, said chip paddle having corners, a circumference and a half-etched section at a lower edge of said chip paddle along said chip paddle circumference.

3. The semiconductor package of claim 2, wherein each of said plurality of tie bars are connected to said corners of said chip paddle.

4. The semiconductor package of claim 3, wherein each of said plurality of tie bars has a half-etched section, and whereas each of said plurality of tie bars externally extend from said chip paddle.

5. A packaged semiconductor, comprising:

a leadframe having a plurality of tie bars, said tie bars having a side surface and a bottom surface, said leadframe having a plurality of dam bars and a space for receiving a semiconductor chip;

a plurality of internal leads connected to said leadframe, said plurality of internal leads having a side surface and a bottom surface, said plurality of internal leads being radially formed at regular intervals along and spaced apart from said circumference of said semiconductor chip and extending towards said semiconductor chip, each of said plurality of internal leads having a half-etched section facing said semiconductor chip, each of said plurality of leads having an upper surface in the plane of said upper surface of said semiconductor chip;

a plurality of conductive wires for electrically connecting to said plurality of internal leads and to said semiconductor chip;

encapsulant material encapsulating said semiconductor chip, said plurality of conductive wires, and said plurality of internal leads to form a package body, wherein flow of said encapsulant material is limited by said plurality of dam bars formed on said leadframe; and

wherein said semiconductor chip, said plurality of internal leads and said plurality of tie bars are externally exposed at respective side and bottom surface.

6. The semiconductor package of claim 5, further comprising:

a semiconductor chip having a planar upper surface, a circumference and a bottom surface secured into said space on said leadframe.

7. The semiconductor package of claim 6, further comprising:

a plurality of input bond pads on the planar upper surface of said semiconductor chip along the circumference and electrically connected to said semiconductor chip; and

a plurality of output bond pads on the planar upper surface along the circumference of said semiconductor chip and electrically connected to said semiconductor chip;

8. The semiconductor package of claim 7, further comprising

a chip paddle connected to said leadframe, said chip paddle having a top surface, a side surface and a bottom surface, said chip paddle bonded to said bottom surface of said semiconductor chip by an adhesive, said chip paddle having corners, a circumference and a half-etched section at a lower edge of said chip paddle along said chip paddle circumference.

9. The semiconductor package of claim 8, wherein each of said plurality of tie bars are connected to said corners of said chip paddle.

10. The semiconductor package of claim 9, wherein each of said plurality of tie bars has a half-etched section, and whereas each of said plurality of tie bars externally extend from said chip paddle.

11. A method for making a semiconductor package, comprising the steps of:

placing a leadframe having a plurality of leads and a space for accommodating a semiconductor chip on an adhesive tape, said plurality of leads having a bottom surface;

affixing a semiconductor chip having a bottom surface, input bond pads and output bond pads within said space on said leadframe;

pressurizing said leadframe and said semiconductor chip downwardly onto said tape;

electrically connecting said input bond pads and said output bond pads of said semiconductor chip to said leads via wires;

encapsulating said semiconductor chip, said wires, and said leads by an encapsulant material to form a package body;

removing said adhesive tape from said package body while leaving said bottom surface of said leads and said bottom surface of said semiconductor chip externally exposed; and

cutting said package from said leadframe.

12. The method as in claim 11, wherein the steps are performed sequentially.

13. A method for making a packaged semiconductor, comprising the steps of:

placing a leadframe having a plurality of leads, a ground ring having a bottom surface, and a space for accommodating a semiconductor chip on an adhesive tape, said plurality of leads having a bottom surface;

affixing a semiconductor chip having a bottom surface, input bond pads and output bond pads within said space on said leadframe;

electrically connecting said input bond pads and said output bond pads of said semiconductor chip to said leads via wires;

encapsulating said semiconductor chip, said ground ring, said wires, and said leads by an encapsulant material to form a package body;

removing said adhesive tape from said package body while leaving said bottom surface of said leads, said bottom surface of said ground ring, and said bottom surface of said semiconductor chip externally exposed; and

cutting said package from said leadframe.

14. The method as in claim 13, wherein the steps are performed sequentially.

15. A method for making a packaged semiconductor, comprising the steps of:

placing a leadframe having a chip paddle having a bottom surface and a plurality of leads on an adhesive tape, said plurality of leads having a bottom surface;

affixing a semiconductor chip having a bottom surface, input bond pads and output bond pads onto said chip paddle via an adhesive;

electrically connecting said input bond pads and said output bond pads of said semiconductor chip to said leads via wires;

encapsulating said semiconductor chip, said wires, and said leads by an encapsulant material to form a package body;

removing said adhesive tape from said package body while leaving said bottom surface of said leads and said bottom surface of said semiconductor chip externally exposed; and

cutting said package from said leadframe.

16. The method as in claim 15, wherein the steps are performed sequentially.